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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/541,092
Filing Date: June 29, 2005
Appellant(s): TOYOZAWA ET AL.

Christopher Tobin
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 7/16/2009 appealing from the Office action mailed 01/28/2009.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,567,066	Hashimoto	05-2003
6,313,819	Maekawa	11-2001
6,091,391	Ling	07-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 17, 18 and 23-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Hashimoto (US 6,567,066).

As to **claim 17**, Hashimoto discloses a display device comprising:

a matrix of pixels, a pixel of said matrix of pixels having an electro-optic material between a pixel electrode and a common electrode (see Col, 6 line 54-Col. 7 line 6);

a common driver having an offset circuit (Fig. 5(14), a common voltage generated by said common driver being applied to said common electrode (see Col. 7 lines 7-28),

wherein said offset circuit is charged to an offset voltage at a time of a rising edge of a power supply voltage (Fig. 5, M1 which is connected to VDD and Fig. 6, offset circuit is charged when M1 is on) said offset voltage adjusting a level of said common voltage (Fig. 6(ΔV)).

As to **claim 18**, Hashimoto discloses the display device as claimed in claim 17, wherein said offset circuit is discharged at a time of a falling edge of said power supply voltage (see Fig. 6, offset voltage ΔVn is discharged at the time of VDD is lowered).

As to **claim 23**, Hashimoto discloses the display device as claimed in claim 17, further comprising:

a vertical driver connected to gate lines of said matrix of pixels (Fig. 1(6));

a horizontal driver connected to signal lines of said matrix of pixels (Fig. 1(3)), said horizontal driver writing a signal voltage to said pixel electrode according to display data (see Col. 4 lines 50-63).

As to **claim 24**, Hashimoto discloses the display device as claimed in claim 23, wherein said level of said common voltage is adjusted with respect to said signal voltage (see Fig. 6(ΔV)).

As to **claim 25**, Hashimoto discloses the display device as claimed in claim 23, wherein said pixel of said matrix of pixels is located at an intersection of one of the gate lines and one of the signal lines (It's inherent to locate pixels at an intersection of gate line and signal line).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto (US 6,567,066) in view of Maekawa et al. (US Patent 6,313,819).

As to **claim 19**, Hashimoto discloses the display device as claimed in claim 18.

However, Hashimoto does not specifically teach wherein said matrix of pixels, said offset circuit, and said start circuit are mounted on an insulating substrate.

Maekawa discloses a liquid crystal display device wherein teaches a display area and a peripheral circuit part for driving the display area are integrally formed in an integrated manner on an insulating substrate (see Col. 4 lines 38-48).

It would have been obvious to one ordinary skill in the art at the time of invention was made to incorporate forming display area and a peripheral circuit on an insulating substrate as in Maekawa into display device of Hashimoto, because circuit complexity can reduced by integration (see Col. 2 lines 38-47).

As to **claim 20**, Hashimoto and Maekawa disclose the display device as claimed in claim 19, wherein said coupling capacitor is mounted on another substrate other than said insulating substrate (see Maekawa Fig. 2(14) and Col. 4 lines 6-15).

As to **claim 21**, Hashimoto discloses the display device as claimed in claim 18, wherein said common driver has a start circuit (Maekawa Fig. 2(15-17)), said start circuit charging a coupling capacitor within said offset circuit to said offset voltage (see Maekawa Col. 3 lines 23-55).

As to **claim 22**, Hashimoto and Maekawa disclose the display device as claimed in claim 21, wherein said start circuit operates only at the time of the rising edge of the power supply voltage and at the time of a falling edge of the power supply voltage, said

start circuit being in a non-operational state during other times (see Maekawa Co. 3 lines 46-64, start circuit only operate during a precharge period, Fig. 3(T1)).

5. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto (US 6,567,066) in view of Ling et al. (US Patent 6,091,391).

As to **claim 26**, Hashimoto discloses the display device as claimed in claim 17, the matrix of pixels being within a display area (see Abstract).

However, Hashimoto does not specifically teach a panel having a peripheral circuit and said display area, said panel being switchable between an operational mode and a standby mode; wherein power consumption by said panel in said operational mode is higher than in said standby mode, driving of said display area being prohibited in said standby mode.

Ling discloses a circuit for LCD which can reduce current consumption, wherein teaches a circuit capable of switching between Execute cycle and IDLE cycle (see Col. 3 lines 11-31).

It would have been obvious to one ordinary skill in the art at time of invention was made to include a switch circuit as in Ling into display device of Hashimoto, because this enable reducing power consumption in idle mode (see Ling abstract).

(10) Response to Argument

1. With respect to rejection claims 17, 18 and 23-25 under 35 U.S.C. 102 as being anticipated by Hashimoto (US 6,567,066).

Regarding claim 17 and 23-25, appellant argues that Hashimoto fails to disclose the offset circuit is charged to an offset voltage at the time of rising edge of supply

voltage. However, examiner respectfully disagrees, based on the scope of claim and broadest reasonable interpretation, Hashimoto's Fig. 5(VDD) reads on "supply voltage", and Fig. 6(ΔV) offset voltage is charged at time of the rising edge off M1 (see Fig. 6, when M1 is switching on, and it is connected to VDD.)

Regarding claim 18, appellant argues that Hashimoto fails to disclose the offset circuit is discharged at a time of a falling edge of power supply voltage. However, Hashimoto clearly shows this in Fig. 6, when at a time of falling edge of power supply voltage (when M1 is switching off), offset voltage ΔV is discharged to 0V.

2. With respect to rejecting claims 19-22 under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 6,567,066 (Hashimoto) in view of U.S. Patent No. 6,313,819 (Maekawa).

Regarding claim 19, appellant argues that Maekawa fails to disclose the presence of an insulating substrate. However, examiner respectfully disagrees, Maekawa teaches a source follower circuit is constructed with a polysilicon TFT (Col. 4 line 18), and it's a well known process in the art that the presence of an insulating substrate in polysilicon TFT fabrication.

Regarding claim 20, Maekawa clearly teaches the coupling capacitor is not mounted on said insulating substrate (see Fig. 2(14) and Col. 4 lines 6-15).

Regarding claim 21, appellant argues that Maekawa fails to disclose a device wherein said common driver has s start circuit, said start circuit charging a coupling capacitor within said offset circuit to said offset voltage. However, examiner disagrees,

Maekawa teaches a start circuit (Fig. 2(15-17)) and start circuit charging a coupling capacitor (see Col. 3 lines 23-55).

Regarding claim 22, Maekawa teaches start circuit only operates during a precharge period (see Col. 3 lines 46-64), hence being in a non-operational state during other time.

3. With respect to rejecting claim 26 under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 6,567,066 (Hashimoto) in view of U.S. Patent No. 6,091,391 (Ling).

Regarding claim 26, appellant argues that Ling fails to teach or suggest driving of display area being prohibited in standby mode. However, examiner disagrees, Ling's disclosure suggests that driving of display area being prohibited in standby mode (Col. 3 line 23-24, “DAC 130 input is set to zero so that it consumes zero current”, this indicates that driving of the display is suspended since the DAC input is set to zero current).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner’s answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/YUK CHOW/

Examiner, Art Unit 2629

Conferees:

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629

/Bipin Shalwala/

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